REMARKS

With claims 1-23 originally pending, with this amendment claims 1, 2, 14 and 23 have been amended as detailed below. Further, claim 19 has been cancelled and new claim 24 has been added.

Section 102 Rejection Based On Miller

Claims 1, 14, 15 and 19-23 stand rejected under 35 U.S.C. §102 as being anticipated by Miller (U.S. Patent No. 6,622,103).

Regarding claim 1, the Office Action with reference to Figs. 3 and 4 of Miller, states that Miller discloses:

> "a variable delay isolation buffer (40) having a signal input (DRIVE), a variable delay control input (Z), and an output (portion connected to node 34); and a delay control circuit (46) having an output (Z) providing the variable delay control input of the variable delay isolation buffer, the delay control circuit setting a delay control voltage potential at its output to control delay through the variable delay isolation buffer to substantially match delay through a time delay reference (column 6, line 30-column 7, line 67)..."

Based on the above amendments and the following remarks, this rejection is now believed to be overcome.

Claim 1 has been amended to claim that the variable delay isolation buffer has a control input "for selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output." Thus, the control input varies the delay of the buffer itself.

Miller, in contrast, discloses in col. 6, lines 27-30 that its buffer 40 is a tri-state buffer that is tri-stated by the input (Z). The Office Action cites the input (Z) of buffer 40 as the variable delay control input of Applicant's claim 1. However, the output (Z) tri-states the buffer output, typically providing a high impedance at the buffer output. The delay of the tri-state buffer will not be affected. Accordingly, claim 1 is now believed allowable as not anticipated by Miller.

Regarding claim 14, the Office Action referring to Figs. 3 and 4 of Miller states that Miller discloses:

> "a tester (10) ... ; isolation buffers (40) having inputs connected in common to a tester (series of TESTER CHANNELS 26), each one of the isolation buffers further having an output (portion connected to node 34); and probes (24) ..."

Based on the above amendments to claim 14, and the following remarks, this rejection is now believed to be overcome.

Claim 14 has been amended to claim "a tester having test channels" and "isolation buffers having inputs connected in common to one of the tester channels." Miller in Fig. 3 shows tester channels (26) separately connected to the isolation buffers, rather than a single test channel connected "in common" to a number of isolation buffers, as now claimed. Accordingly, claim 14 is now believed allowable as not anticipated by Miller.

Regarding claim 15, the Office Action similar to claim 1, cites Miller as disclosing a variable delay control buffer having a variable delay control input (Z) in col. 6 line 30 through col. 7, line 67. This rejection is respectfully traversed.

Claim 15 claims setting a control voltage "to control a time delay of a signal between the input and output of the respective isolation buffer." As indicated above with

respect to claim 1, Miller discloses isolation buffers (40) identified in col. 6, lines 27-30 as tri-state bufferss with a tri-stating input (Z). The tri-stating input (Z) of a tri-state buffer will typically not change the delay from the input-to-output of the tri-state buffer, as claimed in claim 15. Accordingly, claim 15 is believed to be allowable as not anticipated by Miller.

Regarding claims 19 the Office Action states, similar to claim 14, that Miller discloses "distributing a channel through isolation buffers (40) to multiple branches (pins 22 within probe card 20), each branch being connected to one of the plurality of probes." Further, regarding claim 20, the Office Action indicates that controlling delay through the isolation buffers so that each buffer provides the same delay is "considered inherent to Miller because it is the object in Miller to calibrate timing of the tester channels..." This rejection is respectfully traversed.

Claim 20 has been amended to include the elements of claim 19. Claim 19 has, thus, been cancelled. Claim 20 claims "distributing the channel through isolation buffers to multiple branches, each branch being connected to one of the plurality of probes." Miller in Figs. 3 and 4 shows tester channels 26 each only connect by a single buffer (40) to a test circuit (36). Multiple buffers are not connected to a single test channel as claimed. Accordingly, claim 20 is not believed anticipated by Miller.

Further regarding claim 20, although Miller may have an objective of calibrating the timing of the tester channels, as stated in the Office Action, this can be performed in Miller by varying the signals from the tester. Miller does not specifically disclose acomplishing calibration by changing delay through the buffer as now claimed. Accordingly, claim 20 is further believed allowable as not anticiapted by Miller.

Claims 21-23 are believed allowable as not anticipated by Miller based at least on their dependency on claim 19.

Section 102 Rejection Based On Kwon

Claims 19, 20 and 23 stand rejected under 35 U.S.C. §102 as being anticipated by Kwon et al (U.S. Patent 5,070,297, hereafter 'Kwon').

Regarding claim 19, the Office Action referencing Fig. 3 of Kwon states that Kwon discloses:

> "a method of testing integrated circuits ... comprising: supplying test signals from a tester (40) to be distributed from a tester channel (78, 80, 82, 84, 86, 88, 90) to one of a plurality of probes (16) ...; and distributing the channel through isolation buffers (46, 48) to multiple branches (that portion of 16 connected to buffers 46 and 48), each branch being connected to one of the plurality of probes..."

Further, regarding claim 20, the Office Action further indicates that in Kwon:

> "controlling delay through the isolation buffers so that each isolation buffer provides substantially the same delay is considered inherent to Kwon et al. (column 5, lines 56-59.)"

This rejection is respectfully traversed.

As indicated above, claim 20 has been amended to include the elements of claim 19, and claim 19 has been cancelled. Claim 20 claims "controlling delay through the isolation buffers so that each isolation buffer provides substantially the same delay." Kwon in col. 5, lines 56-59 does not disclose changing the delay provided by buffers 46 and 48 in any way. Applicant objects to characterization by the Office Action that varying delay of the isolation buffers is inherent and respectfully requests that if this

rejection is maintained, further reasoning be provided. Accordingly claim 20 is believed allowable as not anticipated by Kwon.

Claim 23 is believed allowable as not anticipated by Kwon based at least on its dependency on claim 19.

Allowable Claims

Claims 2-13 and 16-18 stand objected to as being dependent upon a rejected base claim, but are indicated as allowable if rewritten in independent form. Accordingly, claim 2 has been rewritten in independent form, and is now believed in condition for allowance. Claims 3 and 7-10 are likewise believed allowable in dependent form based on their dependence on claim 2. The remaining claims 4-6, 11-13 and 16-18 are believed allowable in dependent form based on their dependency on claims believed now in condition for allowance as discussed above.

Conclusion

In light of the above amendments and remarks, claims 1-18 and 20-24 are now all believed to be in condition for allowance. Accordingly, reconsideration and allowance of these claims is respectfully requested.

Respectfully submitted,

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